# A LOW-COST PACKAGED MMIC CHIP SET FOR 5.8 GHz ISM BAND APPLICATIONS

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## ABSTRACT

This paper describes a packaged MMIC chip set which was developed for low-cost communication equipment operating in the unlicensed 5.725 to 5.850 GHz Industrial, Scientific, and Medical (ISM) band (FCC rule 15.247). The GaAs MMIC chip set described consists of: 1) Transmit/Receive (T/R) switch, 2) low noise amplifier (LNA), 3) double-balanced downconverter mixer, 4) QPSK/BPSK modulator, and 5) variable-gain medium power amplifier. The MMIC designs are discussed and the measured performance of the packaged chip set is presented.

## INTRODUCTION

The recent allocation of the FCC of spectrum for unlicensed communication applications, commonly known as the ISM bands, have generated a wide range of commercial opportunities for short-range, low-cost telecommunications systems. Some examples include wireless LAN, unlicensed point-to-point communications links, wireless inventory tracking systems, RF identification systems, and short-range personal communications networks, to name a few. The frequency allocations for unlicensed operation -- FCC rule 15.247-- include 902 to 928, 2400 to 2483.5, and 5725 to 5850 MHZ bands. Several manufacturers currently offer low-cost unlicensed radio equipment in the 900 and 2.4 GHz bands; however, due to the unavailability of low-cost RFIC components, the 5.8 GHz band remains largely unexploited. This paper describes the design and measured performance of a low-cost, packaged MMIC chip set that has been developed specifically for 5.8 GHz ISM band telecommunications equipment. For unlicensed operation, the FCC requires the use of spread-spectrum modulation techniques, which can be implemented with direct-sequence (DS) or frequency-hopping radio architectures. A miniaturized, DS spread spectrum radio modem based on this chip set was developed to demonstrate a 5.8 GHz low-cost radio implementation.

## 5.8 GHz MMIC CHIP SET

Figure 1 shows the block diagram of a direct-sequence, spread-spectrum (DSSS) radio front-end designed for 5.8 GHz ISM band applications, indicating the functional

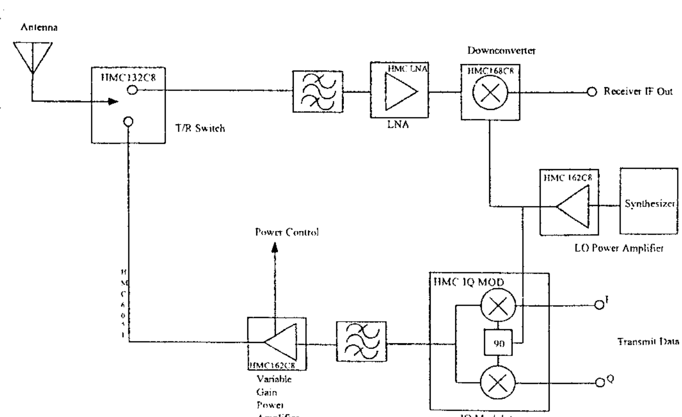


Figure 1. 5.8 GHz ISM band MMIC Chip Set

partitioning of the RFICs. The requirement for a low-cost implementation imposes several design constraints for the chip set, including: 1) single power supply operation (+5 VDC), 2) low-cost, surface-mount packaging, and 3) CMOS logic compatible control pins. A MMIC chip set developed to meet these typical 5.8 GHz ISM band requirements is described in this section.

As shown in Figure 1, the 5.8 GHz MMIC chip set consists of: 1) T/R switch, 2) low noise amplifier, 3) double-balanced mixer, 4) QPSK/BPSK modulator, and 4) variable-gain medium-power amplifier. All MMICs were designed utilizing a 0.5 micron gate-length GaAs MESFET process technology and the chips were packaged into low-cost, surface-mount packages suitable for high volume manufacturing techniques. A photograph of the surface-mount package is shown in Figure 2. The MMIC T/R switch and the double-balanced MMIC mixer have been previously developed [1] and will not be described in detail in this paper.

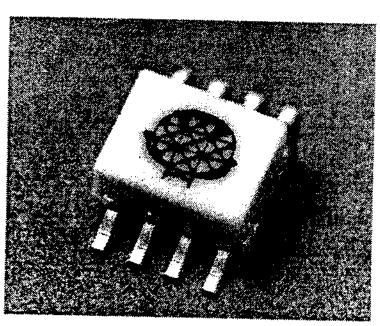

Figure 2. 5.8 GHz Surface Mount Package

Figure 3 shows a photograph of the LNA MMIC chip. Figure 4 depicts the measured gain, noise figure, and input return loss of the packaged part. The LNA is a two-stage, common-source amplifier with four levels (2 bits) of digital gain control. Gain control is achieved with a segmented gate circuit structure in the input stage. A CMOS logic level on the gain control bits effectively determines the transconductance, and therefore gain of the input stage. Since the output stage is operated at a fixed-bias point, the output intercept level remains fairly constant with gain control setting. Gain control is a desirable feature, especially in DSSS systems since it can provide the ability to desensitize the receiver under strong signal conditions such as when the transmitter comes in close proximity to the receiver -- termed the "near-far" problem in CDMA systems. This feature, along with the ability to adjust the transmitter output power as well, can dramatically extend the dynamic range of the communication link.

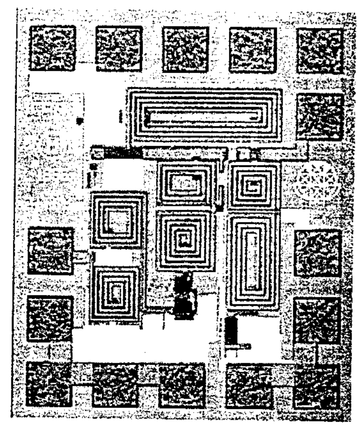

Figure 3. 5.8 GHz MMIC LNA Photograph

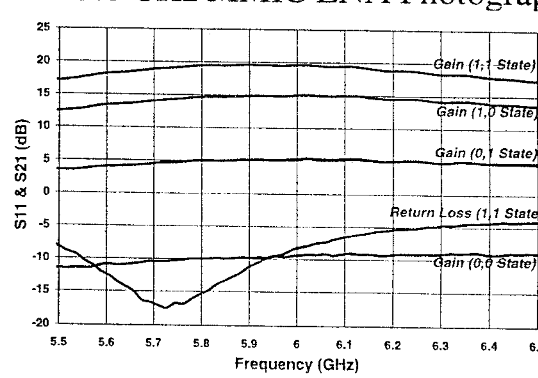


Figure 4a. Measured LNA Gain and Return Loss

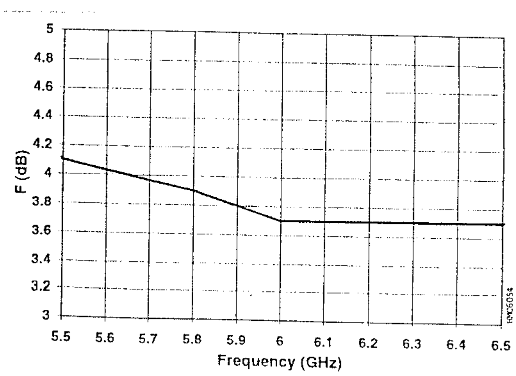


Figure 4b. Measured LNA Noise Figure

A microphotograph of the QPSK/BPSK modulator MMIC is shown in Figure 5. The modulator design consists of an input 90 degree RF hybrid realized with MMIC lumped circuit elements, two double-balanced, switched-FET bi-phase modulators, and an output in-phase combiner. The use of the switched FET double-balanced modulator structure allows for a very high two-tone, third-order output intercept point, typically greater than +20 dBm. This feature reduces the gain requirement in the following power amplifier stage, as well as improves overall transmitter linearity which is important when utilizing QPSK signaling methods. Figure 6 shows the amplitude and phase accuracy of the QPSK modulator for the three symbol states, referenced to the fourth state, indicating a phase balance of approximately +/- 4 degrees and an amplitude balance of approximately +/- 0.5 dB across the 5.8 GHz ISM band. Direct modulation of the transmit carrier significantly reduces the complexity of the transmitter portion of the radio since upconverters and the associated local oscillators and filters are not required; however, this technique will result in increased adjacent channel interference levels (due to the modulation sidelobes) that may be unacceptable in some applications. For BPSK operation, the I and Q modulation ports are tied together. Figure 7 shows the carrier suppression and output sideband level measured performance when operated as a BPSK modulator

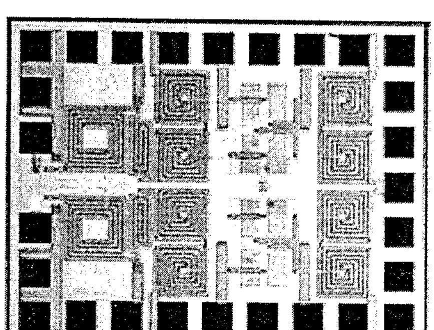

Figure 5. QPSK Modulator MMIC Photograph

(modulation frequency = 2 MHZ). The modulation ports are CMOS logic level compatible and may be connected single-ended or differential.

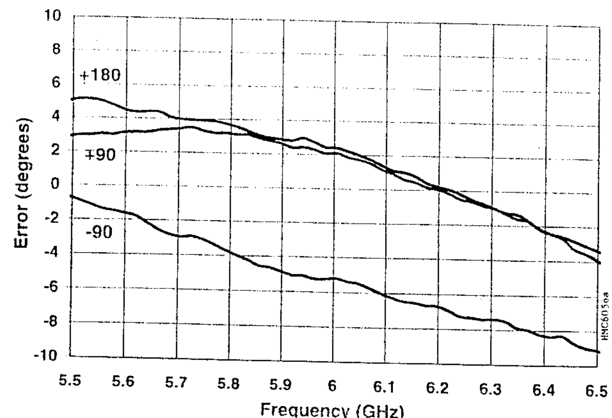


Figure 6a. MMIC QPSK Modulator Measured Phase Error

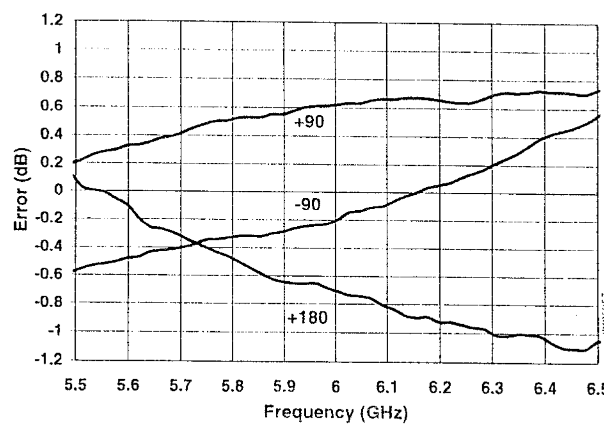


Figure 6b. MMIC QPSK Modulator Measured Amplitude Error

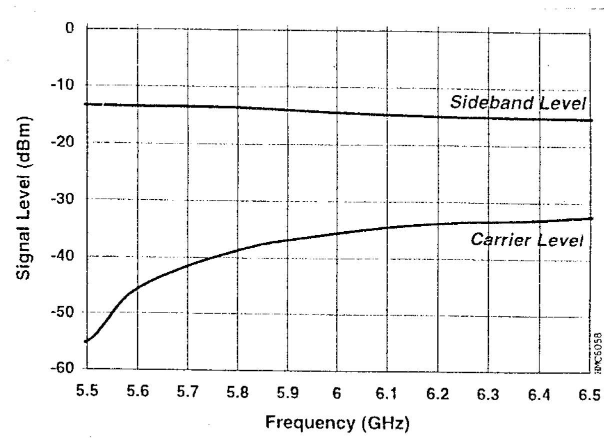


Figure 7. MMIC Modulator Measured Carrier Suppression (BPSK, RF = +0 dBm)

Figure 8 shows a microphotograph of the variable-gain, medium power amplifier (PA) MMIC. The amplifier topology and gain control circuitry is similar to that described for the LNA MMIC; however, the total gate periphery has been increased to provide larger output power capability. Also, since transmitter power settability is typically more important that receiver sensitivity settability, three bits of gain control have been provided. The amplifier may also be used a driver/exciter stage for a high power amplifier stage in long-range communications applications such as point-to-point data links. Figure 9 shows the measured gain versus control settings along with the one dB compression point for the maximum gain setting.

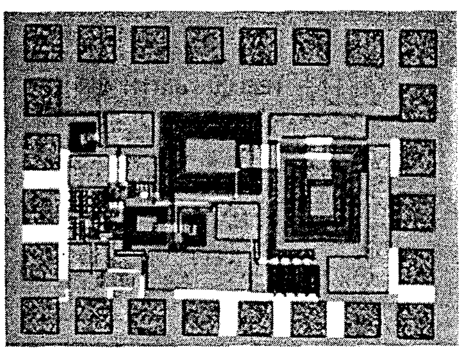

Figure 8. Variable-gain PA MMIC Photograph

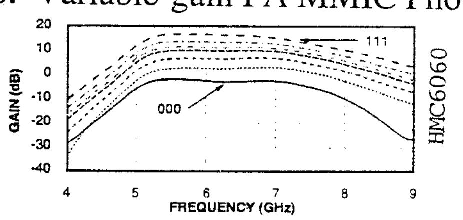


Figure 9a. Variable-gain Power Amplifier MMIC Measured Gain

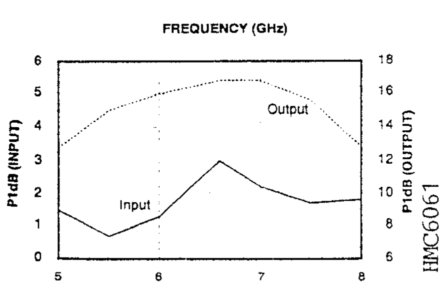


Figure 9b. Variable-gain Power Amplifier MMIC Measured Compression

## SUMMARY

A low cost, packaged MMIC chip set has been developed for 5.8 GHz ISM band unlicensed communication applications. The chip set described consists of: 1) T/R switch, 2) LNA, 3) double-balanced downconverter mixer, 4) QPSK/BPSK modulator, and 5) variable-gain medium power amplifier. The design and measured performance of the chip set has been presented. Future work includes further cost reduction of the chip set by utilizing plastic packaging techniques, and adjusting the circuits for the newly allocated 5.3 GHz band for data communications application.

## REFERENCES

[1] W. Titus, P. Katzin, B. Bedard, “Miniature 3-6 GHz Up and Down Converters”, presented at the 1991 IEEE GaAs IC Symposium, Monterey, California, October 1991.

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